15.7 A 252kgate/71mW Multi-Standard Multi-Channel Video Decoder for High Definition Video Applications

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Multi-standard video decoders play an important role in multimedia applications and motivate the design challenges of reducing both hardware complexity and power consumption in the realization of different video standards. There have been several video decoders [1-5] proposed recently for well-known standards such as JPEG, MPEG, and H.264, which suggests that dedicated hardware is a good solution to low-power implementation for high definition (HD) video applications. A low-cost, low-power multi-standard multi-channel video decoder is presented here that supports JPEG, MPEG-1/2/4, and H.264 for HD video applications. Compared to a state-of-the-art multi-standard video decoder [5] fabricated in 0.13μm CMOS technology, the design can reduce gate-count by 72% and power consumption by 87%, for real-time decoding of HD1080 video.

One solution to realizing low-power video decoders is to reduce the clock rate of external memory accesses, a major component of overall power consumption especially for HD video decoding. The design in [4] used a single external memory with a clock rate of up to 200MHz, and suffers from high power consumption. The designs [1-3,5] used dual external memories to reduce the clock rate for memory accesses (100MHz-to-170MHz), all of which suffer from high IC package cost. Instead, the design presented here reduces memory bandwidth by increasing both the amount of data reuse and the burst length of memory accesses, as well as eliminating cycle overhead in data accesses for supporting HD video decoding with a single AHB-based SDR memory. Figure 15.7.1 shows the system block diagram featuring a hybrid block-level pipelined architecture. Through both datapath and buffer sharing, the functional blocks are optimized, including Hybrid Variable Length Decoder (HVLD), Hybrid Texture Decoder (HTD), Hybrid Pixel Compensator (HPC), and In-Loop Filter (ILF), for carrying out computation for multiple video standards with the same hardware to reduce hardware complexity. To reduce internal memory, the correlated data and pixels of upper neighbors are buffered in external memory through a DMA-like Reusable Data Manager (RDM). To simplify header decoding of bit-streams above the slice layer, a system controller co-operates with an external RISC. Using TSMC 0.13μm 1P8M CMOS technology, real-time multi-standard decoding of HD1080 video is achieved when operating at 120MHz with 71mW power consumption using 252kgates and 4.9KB of internal memory.

Two techniques are used to minimize memory bandwidth for performing pixel compensation, which is the most bandwidth consuming operation in video decoding, as shown in Fig. 15.7.2. The first technique is the *Hybrid block access with cache* for reusing the overlapped data residing at both horizontal and vertical adjacent blocks when supporting the variable block size pixel compensation in H.264, which contributes to 47% of data reuse. The other is the *Dual block access with same MV* for accessing the MPEG/H.264 data blocks with the same motion vector (MV) together, e.g., the luminance blocks Y0 and Y1, Y2 and Y3, as well as the chrominance blocks Cb and Cr, to increase the average burst length of the external memory access operations from 2.18-to-2.75 words/burst to 4.36-to-4.38 words/burst. Combining these techniques together achieves 37% and 56% of bandwidth saving in MPEG-4 and H.264 decoding on HD1080 video, respectively.

The second technique eliminates the overhead cycles associated with the data access in the AHB-based SDR memory through a low latency memory control scheme, as shown in Fig. 15.7.3. The allocated address space is larger than the physical memory size to allow additional bits for sending Mode Control Information (MCI) to the SDR controller seamlessly. The address of the impending burst access operation is pre-calculated based on MCI by an embedded address generator during the current burst access. With the addresses of the impending burst access operation, two techniques are proposed for achieving low memory access latency. One is *Burst Terminates Burst (BTB)* for eliminating the overhead cycles between two consecutive burst access operations by truncating the current burst with a subsequent burst. The other is *Anticipative Row Activation (ARA)* to activate the row of memory banks for the impending access operation in advance, which eliminates the overhead cycles of row activation in the SDR memory. Combining these techniques together contributes approximately a 41% and 38% reduction of memory bandwidth for MPEG-4 and H.264 video decoding, respectively. In summary, applying the proposed techniques in Fig. 15.7.2 and Fig. 15.7.3 achieves the goal of supporting HD video decoding with a single AHB-based SDR memory operating at 120MHz.

Figure 15.7.4 shows the primary technique used to reduce the hardware cost of the proposed design. By observing that most of the operations used in texture coding, intra-prediction, interpolation in inter-prediction, and in-loop filtering can be viewed as filtering operations with fixed coefficients, a *Shared adder-based filter structure* is proposed to realize all the datapaths of 4×4/8×8 IDCT in HTD, intra-prediction and inter-prediction in HPC, and 1-D filter in ILF using only additions and shift operations. First the common terms in realizing these operations are generated and then parallel adder trees are used to compute the output values for the filters. In this way, the common intermediate results are shared to reduce hardware complexity. Using the *Shared adder-based filter structure* contributes 49%, 56%, 64%, and 58% of complexity reduction in 4×4/8×8 IDCT, intra-prediction, inter-prediction, and 1-D ILF filter, respectively.

Figure 15.7.5 summarizes the chip implementation. The core size is 4.2×1.2mm^2 and includes 252kgates and 4.9KB of internal memory. The chip micrograph is shown in Fig. 15.7.7. The power consumption is 71mW@120MHz for real-time HD1080 video decoding. Figure 15.7.6 shows a comparison of this design with state-of-the-art multi-standard and H.264 video decoders for both HD video [1,2,4,5] and portable video [3]. From Fig. 15.7.6, the design outperforms the multi-standard video decoder [5] by 72% in gate-count and 87% in power consumption. Compared to H.264 video decoders [2,4], the design achieves a 34% reduction in power consumption over [2], and a 16% reduction in gate-count as well as 56% reduction in power consumption over [4]. Compared to the MPEG-2/H.264 video decoder [3] for mobile applications, the design achieves a 17% reduction in gate-count. Moreover, it dissipates 7.9mW of power consumption, which is lower than the 12.4mW reported in [3] for real-time H.264 decoding on D1 video, indicating the feasibility for portable video in addition to HD video applications.

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References:
[1] T. W. Chen, et al., "Architecture Design of H.264/AVC Decoder with Hybrid Task Pipelining for High Definition Videos," *IEEE Proc. ISCAS*, vol. 3, pp. 2931-2934, May, 2005.
[2] C. C Lin, et al., "A 160kGate 4.5kB SRAM H.264 Video Decoder for HDTV Applications," *ISSCC Dig. Tech. Papers*, pp. 406-407, Feb., 2006.
[3] T. M. Liu, et al., "A 125μW, Fully Scalable MPEG-2 and H.264/AVC Video Decoder for Mobile Applications," *ISSCC Dig. Tech. Papers*, pp. 402-403, Feb., 2006.
[4] Y. Hu, et al., "A High Definition H.264/AVC Hardware Video Decoder Core for Multimedia SoC's," *Proc. ISCE*, pp. 385-389, Sept., 2004.
[5] H. Y. Kang, et al., "MPEG4 AVC/H.264 Decoder with Scalable Bus Architecture and Dual Memory Controller," *Proc. ISCAS*, vol. 2, pp. 145-148, May, 2004.

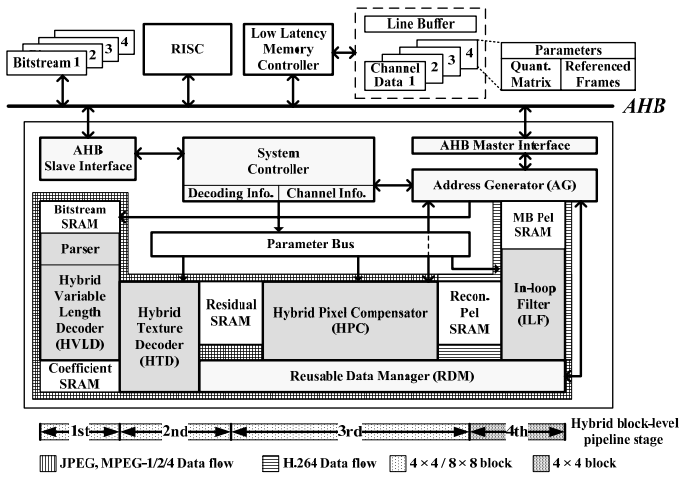

Figure 15.7.1: Block diagram of the multi-standard multi-channel video decoder.

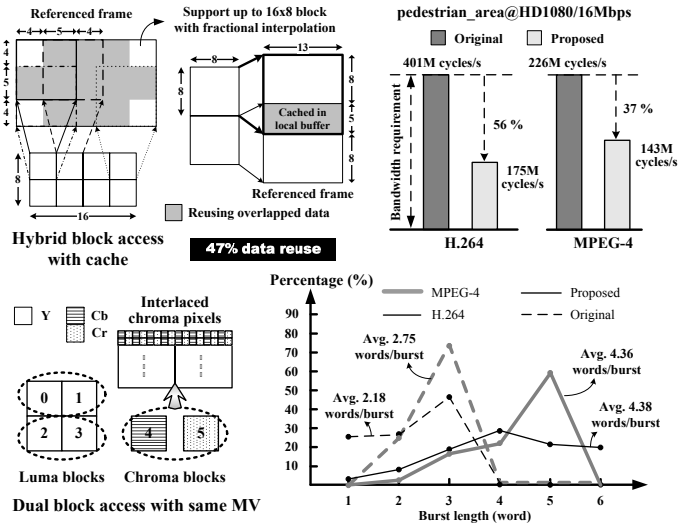

Figure 15.7.2: Optimization techniques for low memory bandwidth.

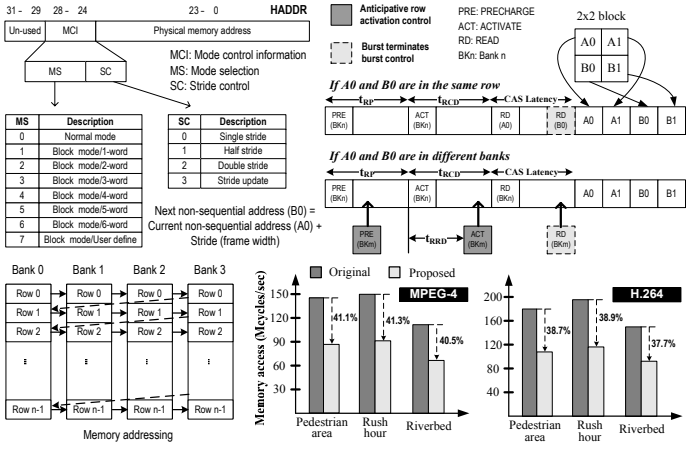

Figure 15.7.3: Optimization techniques for low memory access latency.

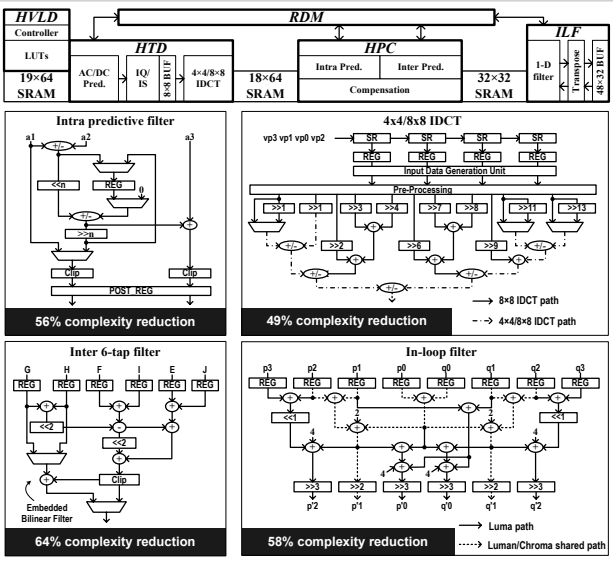

Figure 15.7.4: The major optimization technique for hardware cost reduction.

Name		**Multi-standard multi-channel video decoder**
Technology		**TSMC 0.13μm 1P8M CMOS**
Supply Voltage		**1.2V**
Chip Size (Including PAD)		**5.0 x 2.0 mm²**
Core Size		**4.2 x 1.2 mm²**
Gate Count		**252K (2-input NAND gate)**
On-Chip Memory		**4.9K Bytes (SRAM)**
Operation frequency		**120MHz for HD1080 (1920x1088@30Hz)** **20MHz for 1-ch D1 (720x480@30Hz), 40MHz for 2-ch D1** **6MHz for 1-ch CIF (352x288@30Hz), 12MHz for 2-ch CIF**
Power Consumption	**MPEG-2**	**68.6mW (120MHz@1.0V)** **7.8mW (20MHz@0.8V)** **2.6mW (6MHz@0.7V)**
	MPEG-4	**69.2mW (120MHz@1.0V)** **7.9mW (20MHz@0.8V)** **2.6mW (6MHz@0.7V)**
	H.264	**71.1mW (120MHz@1.0V)** **7.9mW (20MHz@0.8V)** **2.7mW (6MHz@0.7V)**
Package		**160 CQFP**

Figure 15.7.5: Chip specifications and performance summary.

	ISCAS 2005 [1]	ISSCC 2006 [2]	ISSCC 2006 [3]	ISCE 2004 [4] (Conexant)	ISCAS 2004 [5] (C&S, Korea)	This work
Standard	H.264 Baseline	H.264 Main profile	MPEG-2 Simple Profile H.264 Baseline	H.264 Main Profile	JPEG Baseline H.261/H.263 MPEG-4 Simple Profile H.264 Baseline	JPEG Baseline MPEG-1/2 Simple Profile MPEG-4 Simple Profile H.264 Baseline
Specification	2048x1024 @ 30fps	1920 x 1088 @ 30fps	1920 x 1088 @ 30fps	2048 x 1024 @ 30fps	1920 x 1088 @ 30fps	1920 x 1088 @ 30fps
Gate Count	217K	160K	303K	300K	910K	252K
Internal Memory	10KB	4.5KB	2.8KB	74KB	N/A	4.9KB
External Memory I/F	Dual	Dual	Dual	Single	Dual	Single (AHB)
Clock Rate	120MHz	120MHz	100MHz	200MHz	170 MHz	120MHz
Technology	180 nm (1.8V)	180nm (1.8V)	180nm (1.8V)	130nm (1.2V)	130nm (1.2V)	130nm (1.2V)
Power Consumption (HD1080)	N/A	320mW (180nm) 108mW (130nm, post-sim)	N/A	160mW	554mW	71mW@120MHz (1.0V)

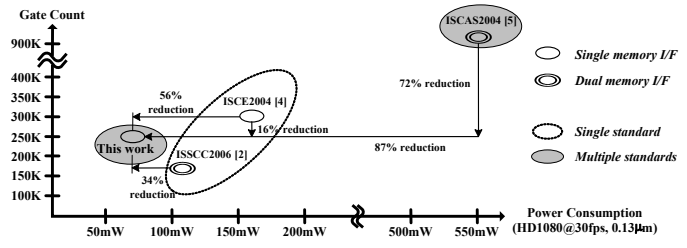

Figure 15.7.6: Comparison with existing designs.

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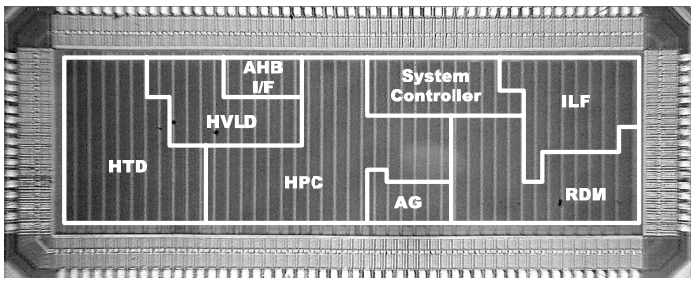

Figure 15.7.7: Chip micrograph.

